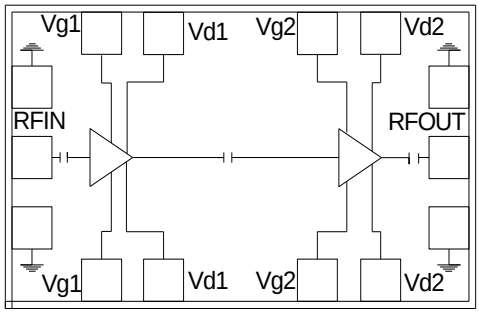
# 9 – 10GHz 12 Watt Power Amplifier

## Features

- **Frequency Range : 9 – 10GHz**
- **41 dBm Psat**
- **24 dB Power gain**
- **36% PAE**
- **High IP3**
- **Dual bias operation**
- **DC decoupled input and output**
- **On Chip Power Detector**
- **0.25 µm InGaAs pHEMT Technology**
- **Chip dimension: 4.8 x 3.9 x 0.1 mm**

**Functional Diagram**




## Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

## Description

The ASL 4037 is a X-band Power amplifier with 41dBm power output. The PA uses 2 stages of amplification and operates in 9 – 10GHz frequency range. The PA features 24 dB of Small Signal Gain. The PA has a high IP3 of 48dBm and 36% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.25µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

## Absolute Maximum Ratings (1)

| Parameter | Absolute Maximum | Units |
|---|---|---|
| Drain bias voltage (Vd) | +8.5 | volts |
| Drain current (Id) | 5.2 | A |
| RF input power (RFin at Vd=8V) | 25 | dBm |
| Operating temperature | -50 to +85 | °C |
| Storage Temperature | -65 to +150 | °C |

**1**. Operation beyond these limits may cause permanent damage to the component

## Electrical Specifications [1] @ $T_A$ = 25 °C, $V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.9V
## $Z_o$ =50 Ω, Pulse Duty Cycle = 10%

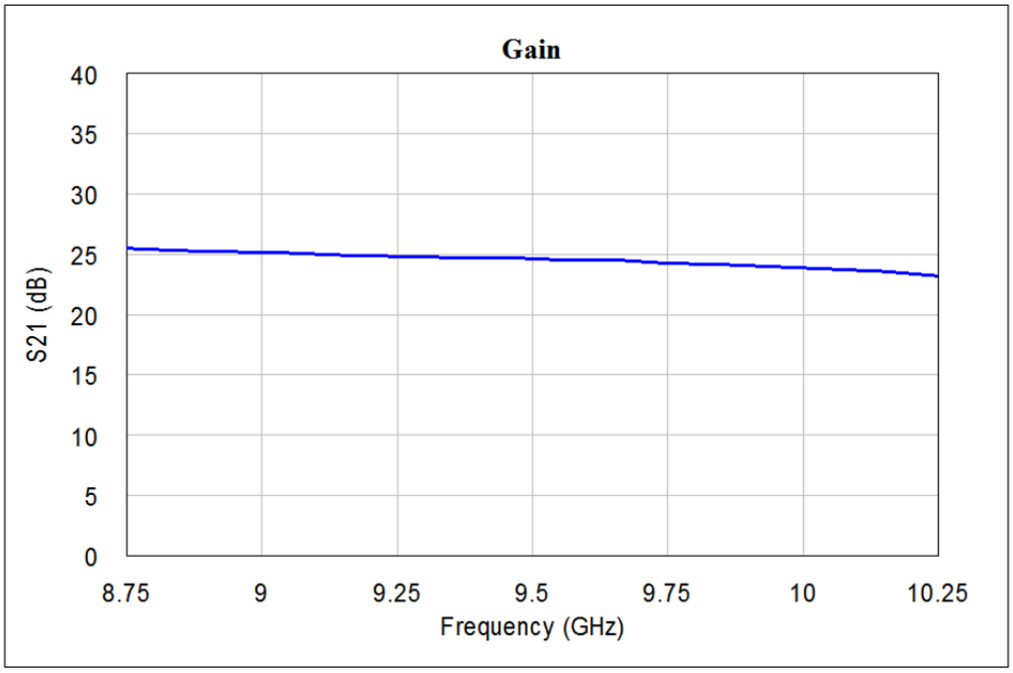
| Parameter | Typ. | Units |
|---|---|---|
| Frequency Range | 9 – 10 | GHz |
| Gain | 24 | dB |
| Gain Flatness | +/-1.5 | dB |
| Output Power (P1 dB) | 40 | dBm |
| Input Return Loss | 9 | dB |
| Output Return Loss | 6 | dB |
| Saturated output power (Psat) | 41 | dBm |
| Output Third Order Intercept (IP3) | 48 | dBm |
| Power Added Efficiency (PAE) | 36% | -- |
| Supply Current($I_{dq}$) | 2.3 | A |

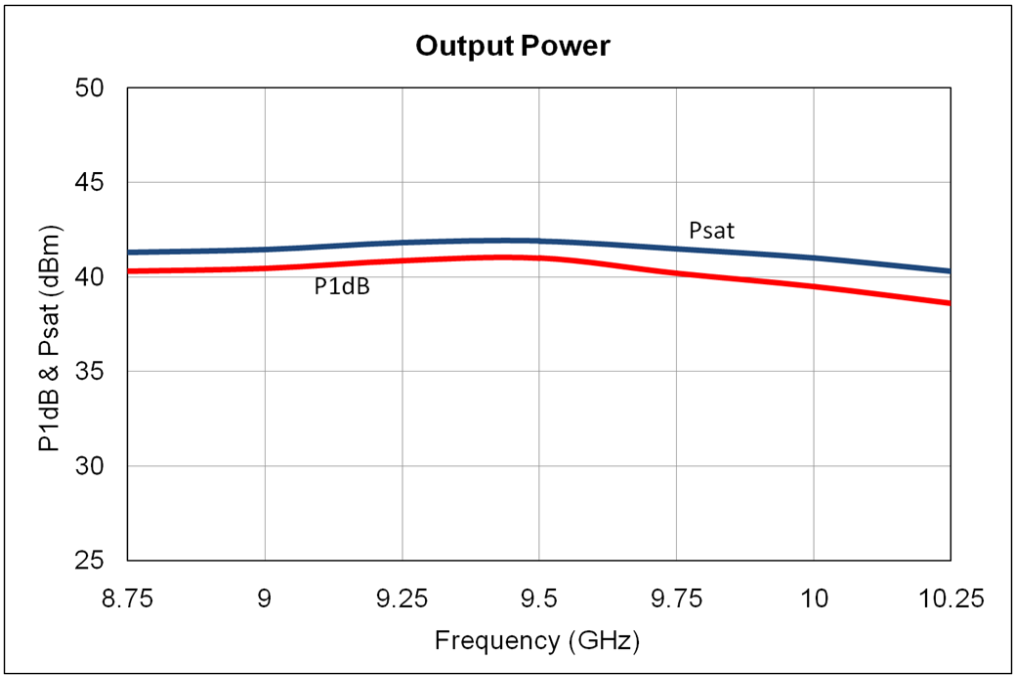
***Note:***

1. Electrical specifications as measured in test fixture.

## Test fixture data

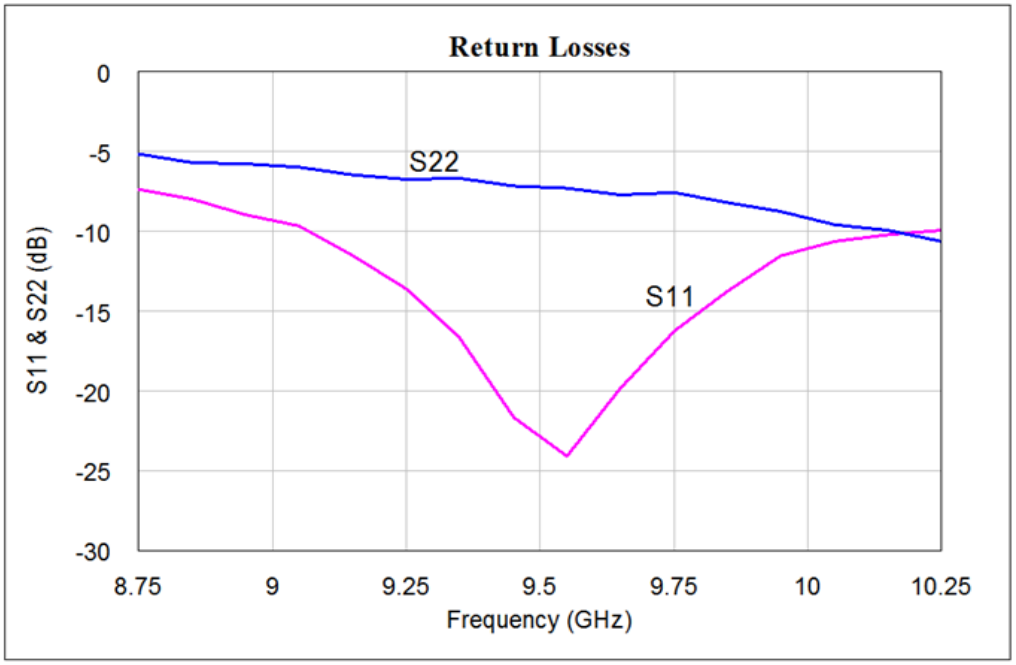
*$V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.9V, Total Current (Idq) =2.3A, $T_A$ = 25 °C, Pulse Duty Cycle = 10%*

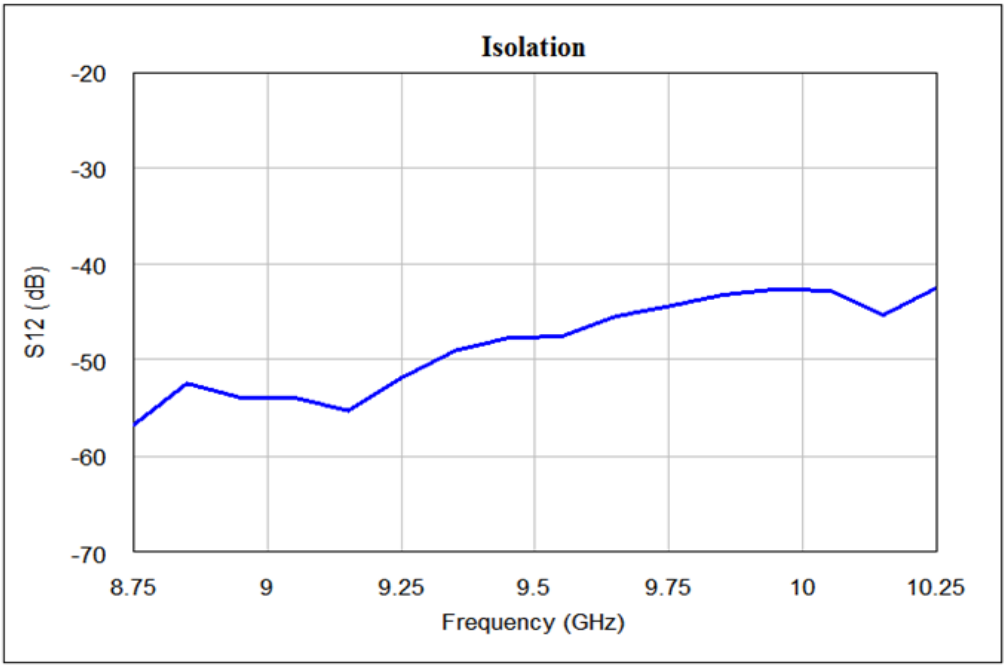


## Test fixture data

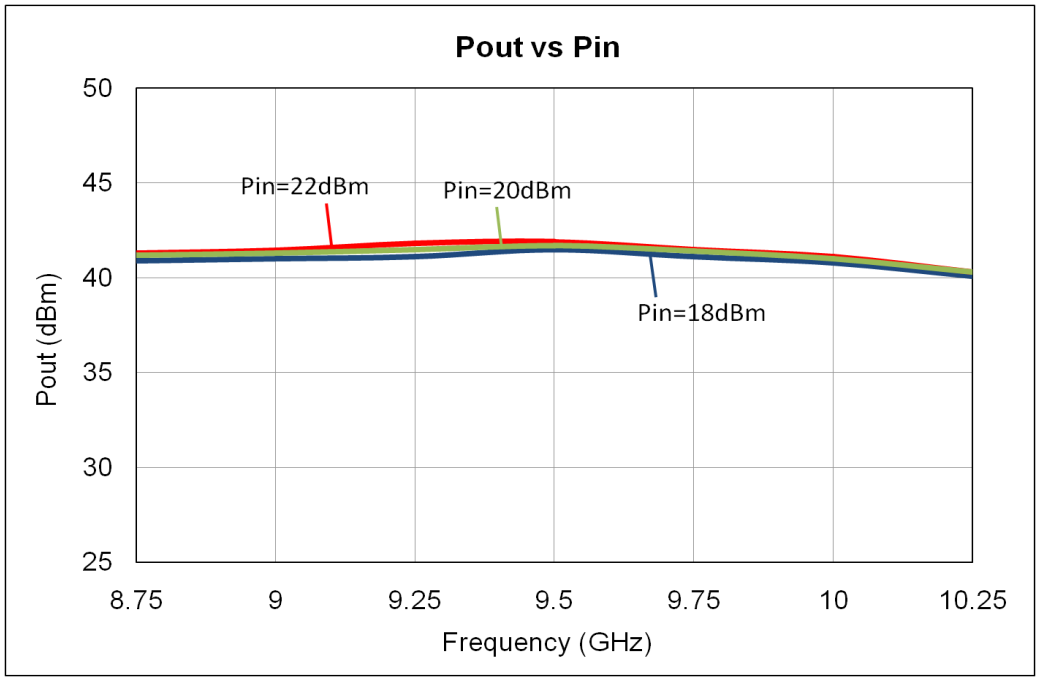
*$V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.9V, Total Current (Idq) =2.3A, $T_A$ = 25 °C, Pulse Duty Cycle = 10%*

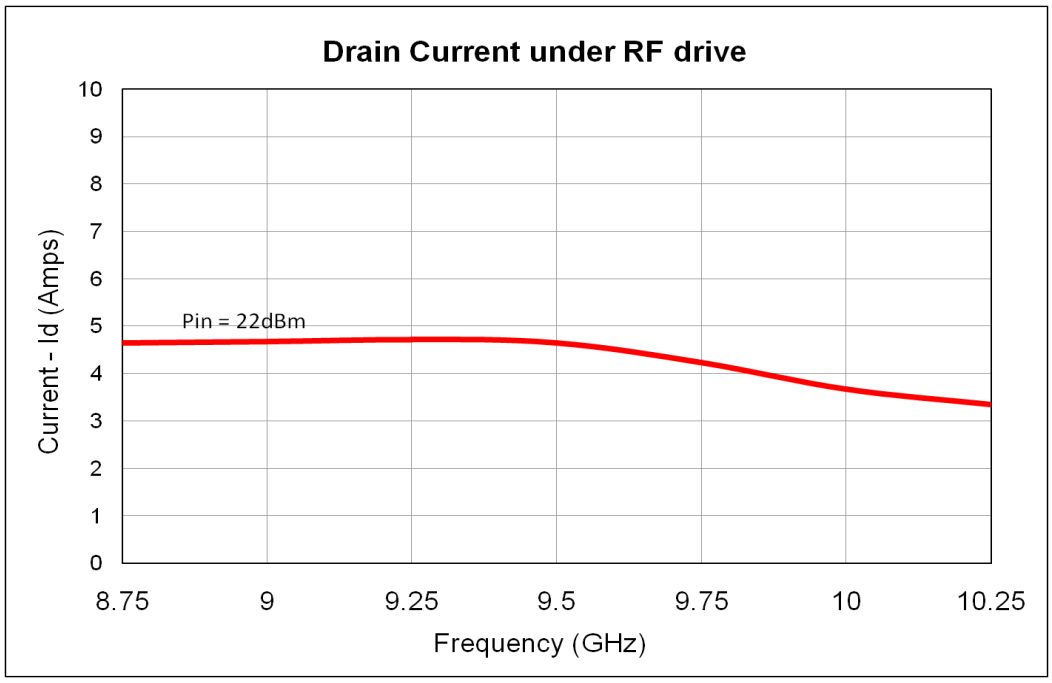


## Test fixture data

*$V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.9V, Total Current (Idq) =2.3A, $T_A$ = 25 °C, Pulse Duty Cycle = 10%*



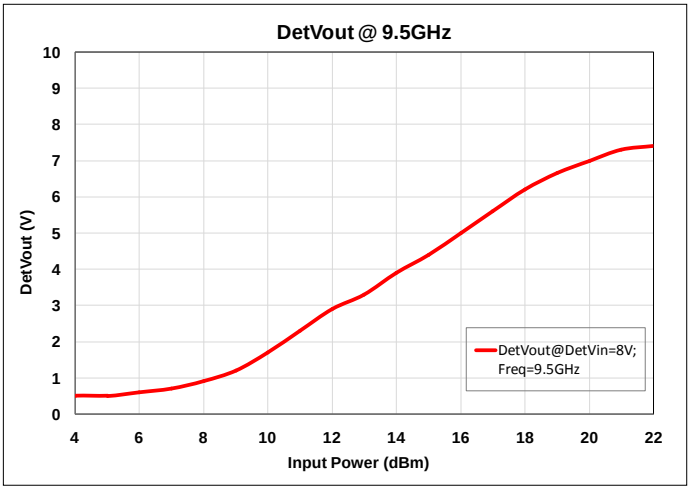
# Power Detector Performance:

## Test fixture data

*$V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.9V, Total Current (Idq) =2.3A, $T_A$ = 25 °C, DetVin = 8V, Pulse Duty Cycle = 10%*

| Pout (dBm) | 9GHz | 9.5GHz | 10GHz |
|---|---|---|---|
| 41dBm | Det Vout = 7V | Det Vout = 7V | Det Vout = 6.7V |
| -30dBm | Det Vout = 0V | Det Vout = 0V | Det Vout = 0V |

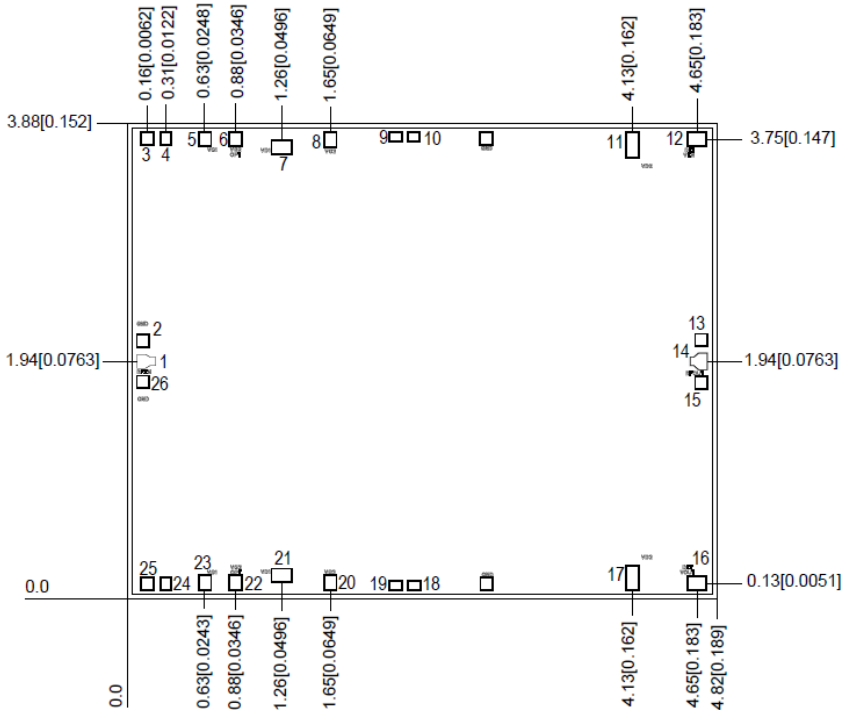
**Description:** The output Voltage of the detector "DetVout" increases with increase in RF output power of the power amplifier. "DetVin" needs to be supplied with 8V in order to activate the detector and the output voltage of the detector is tapped from "DetVout".
The performance of detector with respect to variation of input power of the PA at 9.5GHz is plotted below.




## Off-Chip components used while recording Test Fixture Data:

| Component | Part Number / Description | Vendor |
|---|---|---|
| 100pF SLC Capacitor | D12BV101K5PX/100pF±10%;50V or Equivalent | DLI |
| 1uF MLC Capacitor | 0402G104KXJRW1BC/1uF±10%;16V or Equivalent | Vishay |
| R1=5ohm MMIC Resistor | 1674021/5ohm±5%;1W or Equivalent | AMPL |

## Bond Pad Locations

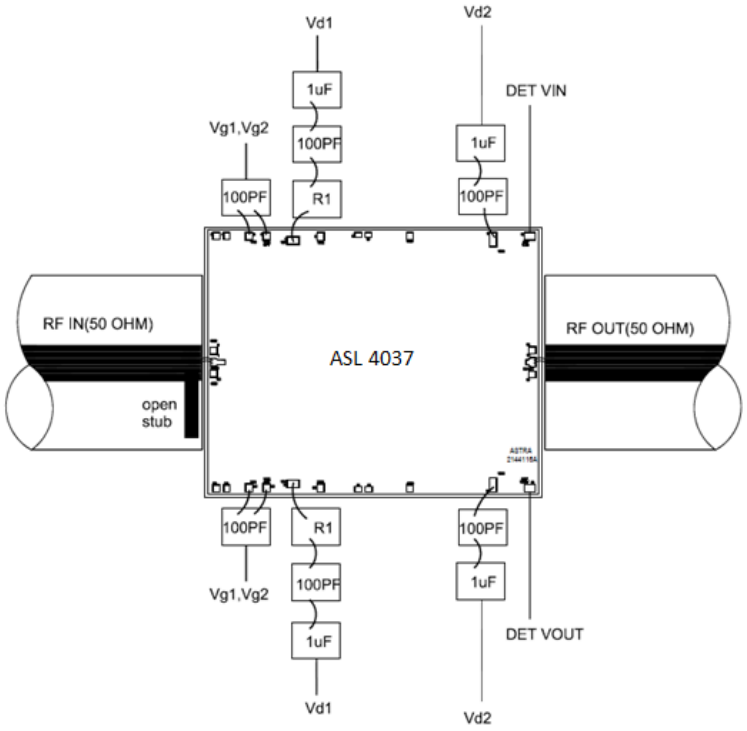



**Units:** millimeters (inches)

**Note:**

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 5,23 : 1st stage gate voltage($V_{g1}$)
4. Pad no. 14 : RF Output
5. Pad no. 7,21 : 1st stage drain voltage($V_{d1}$)
6. Pad no. 6,22 : 2nd stage gate voltage($V_{g2}$)
7. Pad no. 11,17 : 2nd stage drain voltage ($V_{d2}$)
8. Pad no. 12 : Input Voltage for Power Detector (DetVin)
9. Pad no. 16 : Output Voltage for Power Detector (DetVout)
10. All the dimensions shown above are measured taking bottom left corner as reference.

## Recommended Assembly Diagram




**Note :**

1. Open stub of 1mm length, 0.3mm width to be used at Input immediate to the chip for improvement of input return loss as shown in assembly diagram.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
3. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF Single Layer bypass capacitors.
4. Input and output 50 ohm lines are on 5 mil RT Duroid substrate.
5. Apart from 100pF SLC and 1uF MLC Capacitors, higher values of Multi-Layer Capacitors can be used at drain in order to reduce output power pulse droop during pulsed mode of operation.
6. The RF input & output ports are DC decoupled on-chip.
7. This chip is not preferred to be operated under continuous DC voltages, unless it is applied with considerably low drain voltage level.
8. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip.

**Die attach:** Eutectic attachment using fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

**Wire bonding:** For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 to 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

***GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing***

All information and Specifications are subject to change without prior notice.
Before using the product, please download and refer the datasheet from website.